Remarks and Arguments

Claims 1-20 were presented for examination. Claims 1, 5, 6 and 11 have been amended. Claims 10 and 20 have been canceled and claims 21-30 have been added.

The examiner requested that the reference to a co-pending application on page 7 of the specification be updated with the current status of that application. Page 7 has been amended to add the patent number of the U.S. patent corresponding to that application.

The drawings have been objected to under 1.83(a) as not showing a "tree hierarchy" as recited in claims 4 and 6. The tree hierarchy is illustrated in Figures 10 and 12. Note the description at page 31, lines 3-24. Accordingly, this objection is hereby traversed.

Claims 1-20 have been rejected under 35 U.S.C. §112, second paragraph for being indefinite because independent claims 1 and 11 recite the phrase "small enough to avoid rise time problems" which the examiner considers ambiguous. Claims 1 and 11 have been amended to remove this phrase. Accordingly, this rejection is now moot.

Claims 1-7 and 11-17 have been rejected under 36 U.S.C. §103(a) as obvious over U.S. Patent No. 6,092,138 (Schutte) in view of U.S. Patent No. 5,632,021 (Jennings.) The examiner comments that Schutte discloses the invention as claimed with the exception that the reference does not explicitly disclose selectively forwarding transactions. However the examiner asserts that the Jennings reference discloses a tree bus bridge system in which bridges connect different bus segments. Further the examiner asserts that Jennings discloses selectively forwarding transactions and commands based on the bridge memory base register. Consequently, the examiner concludes that it would have been obvious to combine Schutte and Jennings in order to expand the capacity of the system.

The present invention relates to a wired-AND bus bridge that can be used to partition a large wired-AND bus into smaller bus segments. By programming address bitmaps that are internal to each bridge, the various bus segments can be made to appear as one logical bus. The bus bridges are designed to solve two problems which are prevalent in wired-AND bus systems: address number exhaustion and fault isolation.

In accordance with the principles of the invention, bus transactions can be tunneled through a bridge from one bus segment to another bus segment. Tunneling capability provides one way to resolve the address exhaustion problem so common to wired-AND bus implementations. For example, a bus implementation could be created with a number of bus bridges connecting a central wired-AND bus with a number of "island" subsystems. Each wired-AND subsystem could have its own master(s) and slaves, however, the bus addresses used in a given subsystem do not have to be unique relative to the bus addresses used in the other subsystems, nor relative to the addresses used on the central wired-AND bus. The invention allows a master on the main bus to communicate with a bridge connecting the segments using a tunnel command. The tunnel command contains both data and a slave device address that appears as data in the command. Because the slave device address called out by the master appears only as data on the main bus, no slave devices respond even if they have the same address. Therefore, there is no conflict. The command requests that the bridge perform a transaction on a subordinate bus at the slave address. When the bridge receives the tunnel command it extracts the data and the slave address and forwards the data to the slave address.

The present invention also addresses the fault isolation problem so that a fault on one level of bus hierarchy does not render the whole bus useless. For example, a common wired-AND bus system is an I^2C bus system. An I^2C bus is either BUSY or IDLE, depending on whether a START or STOP condition was most recently issued by a bus master. There are no timeouts associated with transaction duration, so a master that starts a transaction (with a START condition on the bus) but does not terminate it with a STOP condition (for example, because the master crashed or was hot-removed) will leave the bus perpetually in the "busy" state as far as all the devices on that bus are concerned. In accordance with the principles of the invention when a bus master is driving a transaction through the inventive bridge to a subsystem on the other side, if the remote bus is "hung" as described above, the bridge will time-out after a programmable duration, reset the remote bus, and then allow the original transaction to pass through.

In addition, in accordance with the principles of the invention, a "hard" fault on a subordinate bus will not cause a fault on a main bus. For example, if a master on a main bus accesses a device address on a subordinate bus, and if that subordinate bus is hard-faulted, such as from a hardware short on the clock or data lines, the bridge can still inform the master by means of a negative acknowledge (NAK) that a problem exists on the subordinate bus. Thus, the master knows that it cannot communicate with the specified device address. Further, the master knows roughly where the hardware fault exists, i.e. on the subsystem behind the bridge.

In order to particularly point out these differences, claim 1 has been amended by including the limitations of claim 10 to recite the inventive tunnel command. For example, amended claim 1 now recites, in lines 12-17, "sending a tunnel command from a bus master on the first bus segment, the tunnel command containing data and a device address of the other slave device as data, to a bus bridge connecting the first and second bus segments whereupon the bridge extracts the slave device address and forwards the data to the extracted slave device address on the second bus segment."

The bus bridge described in the Schutte reference is designed to isolate wired-AND bus segments in order to solve a capacitance loading problem. In particular, in order to provide a high speed message transfer mode, Schutte uses a special load circuit that supplies additional current to the bus allowing the load resistor to more quickly pull the bus to the quiescent level. However, since not all I^2C devices can operate in this special high speed mode, a bridge circuit is used to connect a high speed bus segment to a non-high speed bus segment. The bridge circuit either connects the two bus segments together when both segments are operating in normal speed mode or disconnects the segments when one segment is operating in high speed mode. However, with the exception that some of the master devices can drive increased currents on the clock and data lines, all of the master devices disclosed in Schutte are conventional devices and there is no disclosure of any special commands in which an address is treated as data when the command is generated and then extracted by the bridge. Thus, Schutte does not address the address exhaustion problem solved by the present invention.

The Jennings references discloses a PCI bus system. As is well-known, a PCI bus is "auto-configuring", with addresses being dynamically allocated. See for example, on the World Wide Web, the address tldp.org/LDP/tlk/dd/pci.html for a more detailed discussion of address assignment in a PCI system. Because address are hierarchically assigned in a PCI system, address exhaustion is generally not a problem. Consequently, Jennings discloses no solution for dealing with this problem. Consequently, Jennings combined with Schutte cannot disclose or suggest a tunnel command along the lines recited in amended claim 1.

Claim 10 was originally rejected over the combination of Schutte and Jennings further in view of U.S. Patent No. 6,594,712 (Pettey.) The examiner asserts that the combination of Schutte and Jennings does not explicitly disclose slave devices with the same addresses, but that such slave devices are disclosed in Pettey. While Applicant agrees that Pettey does disclose two slave devices with the same address in an Infiniband system (as described in the present specification), Pettey does not disclose a method or apparatus to deal with the two addresses. In particular, it does not disclose the tunnel commands recited in amended claim 1 nor any equivalent thereof. Thus, its combination with Schutte and Jennings cannot teach or disclose the tunnel command recited in amended claim 1.

Claims 2-7 are dependent, either directly or indirectly, on amended claim 1 and incorporate the limitations thereof. Therefore, they distinguish in the same manner as amended claim over the cited references. Claims 5 and 6 were amended to accommodate the changes to claim 1.

Claim 11 has been amended in a similar manner as claim 1 and distinguishes over the cited references in the same manner as claim 1.

Claims 12-17 are dependent, either directly or indirectly, on amended claim 11 and incorporate the limitations thereof. Therefore, they distinguish in the same manner as amended claim over the cited references.

Claims 8-9 and 18-19 have been rejected under 35 U.S.C. §103(a) over Schutte in view of Jennings and further in view of U.S. Patent No. 5,546,546 (Bell.) The examiner asserts that the combination of Schutte and Jennings discloses the claimed subject matter that it does not explicitly disclose a bridge ID. The examiner asserts that

Bell discloses such a bridge ID and that the combination of Bell with Schutte and Jennings would have been obvious in order to maintain transaction order in a bridge system. It is noted that the bus specifically mentioned in the Bell disclosure is a PCI bridge. Other busses are mentioned in passing including EISA, ISA or VESA busses. (See Bell, column, 7, lines 53-57. As discussed above, the address exhaustion problem addressed by the present invention does not arise in these bus systems because the bus addresses are dynamically assigned. Consequently, Bell can add nothing to the combination of Schutte and Jennings which would teach or suggest the claimed tunnel command in amended claim 1 on which claims 8-9 depend, or in amended claim 11, on which claims 18-19 depend. Thus, claims 8-9 distinguish over the cited combination of Schutte, Jennings and Bell in the same manner as amended claim 1 and claims 18-19 distinguish over the cited combination of Schutte, Jennings and Bell in the same manner as amended claim 11.

Claims 10 and 20 have been rejected under 35 U.S.C. §103(a) over Schutte in view of Jennings and further in view of Pettey. This latter reference is discussed above in connection with the rejection of claims 1 and 11.

New claims 21-30 have been added to specifically cover the fault isolation aspects of the current invention. In particular, claims 21-25 recite a method of constructing a multi-segment wired-AND bus system in which a bus bridge connecting two bus segments performs fault isolation when a bus master is driving a transaction through the inventive bridge to a subsystem on the other side. In particular, if the remote bus does not respond within a predetermined time, the bridge attempts to cause a device connected to the second bus segment to respond. If the device responds then, the bus is reset. If the device does not respond, then the bus is permanently hung and the bridge so informs the bus master. This operation is described in the present specification at page 28, line 17 to page 29, line 9. Claims 26-30 are apparatus claims containing limitations equivalent to those set forth in claims 21-25.

The bus bridge in Schutte does not provide bus fault isolation, so that a fault on one level of bus hierarchy will render the whole bus useless when the bus bridge connects the bus segments together. The other references describe bus systems in

which the bus "hanging" problem does not occur and, thus, cannot teach or suggest a solution as recited in claim 21-30.

Based on the above discussion, claims 1-9, 11-19 and 21-30 are allowable and advancement of this application to issue is respectfully requested. The Commissioner is hereby authorized to charge any fees or credits under 37 C.F.R. §1.16 and 1.17 to our deposit account No. 02-3038.

Respectfully submitted

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